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Intel's 45nm CMOS Technology Performance Parameters in VLSI Design

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Abstract **- In this paper we describe Intel's 45nm technology performance parameters and relate it with a other technology.**

Firstly, we give an overview of the evolution of important parameters such as the integrated circuit (IC) complexity, gate length, switching delay and supply voltage with a prospective vision down to the 22 nm CMOS technology.

Keywords **- Hafnium-Based High-K (Hi-K) Gate, 45nm Transistor.**

I. Introduction

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area. Table (a) gives an overview of the key parameters for technological nodes from 180 nm, introduced in 1999, down to 22 nm, which is supposed to be according to Moore's Law & in production around 2011. Demonstration chips using 45-nm technology have been reported starting in 2004. Mass market manufacturing with this technology is scheduled for late 2007.

Technology Node (nm)	130 nm	90 nm	65 nm	45 nm	32 nm	22 nm
First Production	2001	2003	2005	2007	2009	2011
Effective gate length	70nm	50nm	35 nm	25 nm	17 nm	12 nm
Gate material	Poly	Poly	Poly	Metal	Metal	Metal
Gate Dielectric	SiO_2	SiO_2	SiON	HiK	Hi-K	Hi-K
Kgates/mm^2	240	480	900	1500	2800	4500
Memory point (μ^2)	2.4	1.3	0.6	0.3	0.15	0.08

Table (a)

In January 2007, Intel introduced one of the biggest advancements in fundamental transistor design in 40 years - the use of dramatically different transistor materials (a new material combination of hafnium-based high-k (Hi-k) gate dielectrics and new metal materials for the gate) to build the hundreds of millions of microscopic 45nm transistors inside the next generation of the company's Intel Core 2 processor family. By using the element Hafnium, a metal that significantly reduces electrical leakage and provides the high capacitance necessary for good transistor performance.

In the second half of 2007, Intel will begin production of the next generation Intel® Core™2 process family code named "Penryn" which is based on our industry-leading 45-nanometer (nm) Hi-k metal gate process technology and latest micro architecture enhancements. This next evolution in Intel Core™ micro architecture builds on the tremendous success of our revolutionary micro architecture (currently used in both the Intel® Xeon® and Intel® Core™2 processor families) and marks the next step in Intel's rapid cadence for delivering a new process technology with an enhanced micro architecture or an entirely new micro architecture every year.

With more than 400 million transistors for dual-core processors and more than 800 million for quad-core, the 45nm Penryn family introduces new micro-architecture features for greater performance at a given frequency, plus expanded power management capabilities for new levels of energy efficiency. The 45nm Hi-k next generation Intel Core 2 and Intel Xeon processors have more transistors but are about 25 percent smaller in silicon area than Intel® s current 65nm products and operate at the same or lower power than the current Intel Core 2 processors.

The Penryn family adds to the Intel Core 2 processor Family:

- A second-generation quad-core desktop processor with up to 12MB L2 cache.
- A new dual-core desktop processors with up to 6MB shared L2 cache.
- A new low-power dual-core mobile processor with up to 6MB shared L2 cache and a new low-power state that substantially lowers processor idle power.

The Penryn family also adds several new processors to the Intel Xeon processor family:

- A second-generation quad-core dual-processing (DP) server/workstation processor with up to 12 MB L2 cache.
- A dual-core DP processor with 6MB shared L2 cache.
- A multi-processing (MP) quad-core processor currently under development.

II. Remarkable Performance Improvements

The Penryn family includes a number of improvements to help speed up software and improve response times.

1. Micro architecture optimizations

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New optimizations increase the overall performance and energy efficiency of the already leading Intel® Core™ micro architecture to deliver more instruction executions per clock cycle. This means more performance and quicker computer responsiveness.

2. Enhanced Intel® Virtualization Technology

Penryn micro architecture improvements speed up virtual machine transition (entry/exit) times by an average of 25 to 75 percent. (Requires no virtual machine software changes.)

3. Higher Frequencies

Penryn processors deliver higher core and bus clock frequencies within existing power and thermal envelopes to further increase performance. Desktop and server products will introduce core speeds greater than 3GHz.

4. Fast Division of Numbers

Penryn processors provide faster divider performance, roughly doubling the divider speed over previous generations for computations used in nearly all applications through the inclusion of a new, faster divide technique called Radix 16.

5. Larger Caches

Penryn family processors include up to a 50 percent larger L2 cache with a higher degree of associativity to further improve the hit rate and maximize its utilization. Cache is a memory reservoir where frequently accessed data can be stored for more rapid access. Larger and faster cache sizes speed a computer's performance and response time.

6. Unique Super Shuffle Engine

Implementing a full-width, single-pass shuffle unit that is 128-bits wide, Penryn processors can perform full-width shuffles in a single cycle. This significantly improves performance for SSE2, SSE3 and SSE4 instructions that have shuffle-like operations like pack, unpack, and wider packed shifts.

7. Streaming SIMD Extensions 4 (SSE4) Instructions

The Penryn family includes Streaming SIMD Extensions 4 (SSE4) instructions, the most significant SIMD instruction set addition since the original SSE Instruction Set Architecture (ISA). This extends the Intel® 64 instruction set architecture to expand the performance and capabilities of the Intel® architecture.

8. Intel® Dynamic Acceleration Technology

For the mobile Penryn processor, Intel has enhanced the Intel® Dynamic Acceleration Technology available in current Intel Core 2 processors. This feature uses the power headroom freed up when a core is made inactive to boost the performance of another still active core.

9. Deep Power Down for energy savings and improved battery Life

The mobile Penryn processor has a new advanced power management state called Deep Power Down Technology that significantly reduces the power of the processor during idle periods such that internal transistor power leakage is no longer a factor. This helps extend battery life in laptops and is a major advancement over previous generation industry-leading Intel mobile processors.

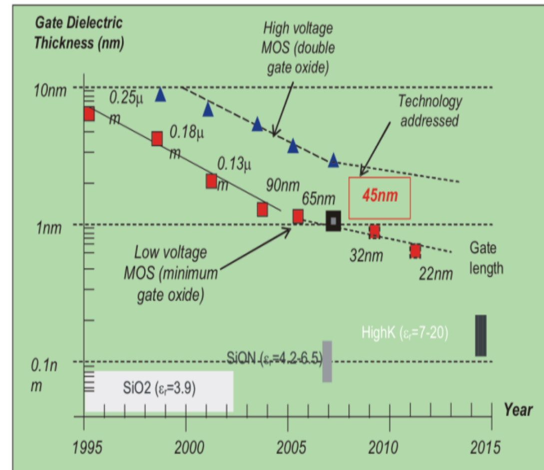

Fig.(a). Technology scale down to nano-scale device

III. 45nm Transistors

A 45nm technology is used in manufacturing VLSI transistor which has used in both the Intel® Xeon® and Intel® Core™2 processor families. Figure shows the constructional view of 45nm transistor with 50nm gate. (made up of SiO_2) This type of technology increases the switching speed of the transistor as compared to the previous VLSI technology.

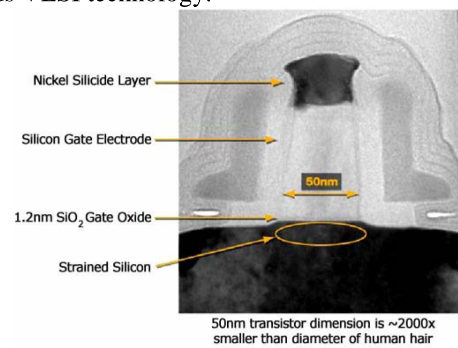

Fig.(b): 45nm Transistor

Some of the key features of the 45 nm technologies from various providers are given in Table (b).

Parameter	Value
V_{DD} (V)	0.85-1.2 V
Effective gate length (nm)	25-40
Ion N (µA/µm) at 1V	750-1000
Ion P (µA/µm) at 1V	350-530
Ioff N (nA/µm)	5-100
Ioff P (nA/µm)	5-100
Gate dielectric	SiON, HfO2
Equivalent oxide thickness (nm)	1.1-1.5
No. of metal layers	6-10
Interconnect layer permittivity K	2.2-2.6

Table (b)

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IV. Recent ICs

- *Intel Dual-Core Processor*
  45nm, More than 400 million transistors, 2.8 GHz.
- *Intel Quad-Core Processor*
  45nm, More than 800 million transistors, 2.4 GHz.
- *Intel Itanium 2*
  90 nm, 1.7 billion transistors, 1 GHz.

V. New Technologies New Challenges

a) Power Consumption

Optimization of power, but still want high performance circuit with more features. Glitches were never look with perspective of power but now you cannot ignore them.

b) Packing

Placing every transistor of circuit on smallest area possible is Herculean task, and then everyone has to be routed.

c) Verification

Today's designs require advance testability circuit just to ensure correct manufacturing. More no. of verification teams than design team.

d) Dealing with leakage problems

This generation problem, as if Ioff = 1 nA, so even if a 500 million transistor are OFF, still will leak 0.5 Amperes.

e) Routing Problems

While transistor scaling ensures we can pack more in the same area, however an efficient metal stack is required to wire all these transistors.

f) Cross talk, Yield

Metal width and pitches are reducing, and additional layers of metal are being added. The reduction of metal width causes increased resistance. This leads to increased coupling capacitance which results in more crosstalk between signal lines.

Yield is a metric of manufacturability, but is not limited to process defects. Today, yield can be impacted by crosstalk which could cause glitches on data or clock resulting in intermittent failures which can be impossible to debug if not caught early in the design.

VI. Acknowledgement

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